REMARKS/ARGUMENTS

This Amendment is in response to the Office Action dated April 14, 2004.

Claims 1-15 are pending in the present application. Claims 1-15 are rejected.

Claim Objections

The Examiner states,

> **2. Claim 9 objected to because of the following informalities: There are two colons ":" ending the preamble. Appropriate correction is required.**

Applicant has amended claim 9 to make the appropriate correction.

Claim Rejections – 35 USC 112

The Examiner states,

> **3. Claims 3 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation "at least one point of interest" is indefinite and does not clearly define "what" is the point of interest. More clarification is required.**

Applicant has amended claims 3 and 11. Claims 3 and 11 particularly point out and distinctly claim the subject matter that applicant regards as the invention.

> **4. Claims 6 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which application regards as an invention. The limitation "signals of interest" is indefinite and does not clearly define "what" are the signals of interest. More clarification is required.**

Applicant has amended claims 6 and 13. Claims 6 and 13 particularly point out and distinctly claim the subject matter that applicant regards as the invention.

5. Claim 9 recites the limitation "the at least one bus" in the debug client function. There is insufficient antecedent basis for this limitation in the claim. The limitation should read "a at least one bus" or "at least one bus".

Applicant has amended claim 9 to make the appropriate correction.

6. Claims 10-15 are rejected because they depend on claim 9 and contain the same problems of indefiniteness.

Claims 10-15 are definite for the same reason that claim 9 is definite.

Claim Rejections – 35 USC 103

The Examiner states,

7. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. Pat. No. 6,260,087), or Chang1, in view of Barnett (U.S. Pat. No. 6,173,419) and further in view of Change (U.S. Pat. No. 5,687,325) or Chang 2.

Claim 1:

Chang 1 teaches in Fig. 1, a PCI Bus Controller ("PCIBC") ASIC 10 (ASIC). Chang1 also teaches included in the PCIBC 10 are conventional functional blocks (standard cell including a plurality of logic functions) include a SRAM block 12, an EEPROM or Flash Memory block 14, a FIFO block 16, a RISC processor or DSP block 18, and a PCI bus interface block 22 (internal bus with internal signals). In principle, the RISC processor or DSP block 18 can be any type of central processing unit ("CPU") including a DSP, a micro-controller, RISC or a complex instruction set computer ("CISC"). (Col. 5, lines 33-43). Chang1 also teaches the PCIBC 10 includes programmable logic block (PLB) 26 (a FPGA function). (Col. 5, lines 56-58). Chang 1 does not explicitly teach that the PIB 26 has a debug function, however, Chang1 does suggest that the PLB 26 can implement one or more functions that is performed by the functional blocks included in the PCIBC 10. (Col. 5, lines 65-067; col. 6, lines 1-5). As previously mentioned, Chang1 also discloses a RISC processor or DSP block 18 which can be any type of central processing unit ("CPU") including a, a micro-controller. Chang1 further teaches a Smart Card Controller ("SCC") ASIC IN Fig. 2. Barnett teaches an emulator that may be used to emulate a micro-controller in a smart card. FPGA 100 is programmed with a model of a micro-controller 102 and a model of monitoring or debut log 104 (debug client function). Col. 5, lines 37-43). Barnett further teaches monitoring or debug logic 104 provides the logic surrounding micro-controller 102 that allows a fully transparent window into the internal functioning of micro-

controller 102 and observe the signals and timing at any point in the micro-controller (observe signals). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chang1's PLB 26 program with Barnett's debug function in FPGA 100 to observe signals. The artisan would be motivated to do so because it would enable Chang1 to have more control of the micro-controller in observing the signals and timing at any point. Chang2 teaches of a FPGA included within an ASIC that is configurable to effect a special digital logic circuit interconnection between fixed functional units (manipulates bus signals). Col. 3, 32-37; col. 5, lines 66, 67; col. 6, lines 1-19). It would have been obvious to one of ordinary skill in the art at the time the invention was made to also configure Chang1's PLB 26 as Chang2's FPGA to manipulate the signals of the Chang1's conventional functional blocks. The artisan would be motivated to do so because it would enable Chang1 to have more control of the micro-controller in manipulating the data presented in Chang2's bus interface 26.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim limitations. MPEP § 2142.

First, there is no suggestion or motivation to combine Chang 1 and Barnett. Although the Examiner states "The artisan would be motivated to [combine the references] because it would enable Chang1 to have more control of the micro-controller in observing the signals and timing at any point," Barnett contradicts this position. In Barnett, an emulator is used to debug software operating on a target micro-controller in a target circuit environment. (Abstract) An emulator is a non-intrusive software debugging tool that uses external hardware to provide transparent operation of a microprocessor embedded in a target circuit. The emulator microprocessor *substitutes* for the target microprocessor during target circuit testing and execution, and the emulator traces all activity that occurs *at the target microprocessor.* Col. 3 line 63 - col. 4 line 1. The emulator is programmed into a field programmable gate array (FPGA) which will work in real time, *does not need to be fabricated as an expensive ASIC*, and is programmable to

other configurations. Col. 5, lines 34-36. It seems clear that Barnett specifically teaches against using an emulator as an ASIC (claim 1 is directed towards an application specific integrated circuit (ASIC)). Furthermore, Barnett teaches that an emulator should substitute for the microcontroller for testing purposes, not be "coupled to the at least one bus and plurality of internal signals . . . that observes and manipulates the at least one bus and the plurality of internal signals."

Additionally, there is no suggestion or motivation to combine Chang 2 and Chang 1. Although the Examiner states that it would have been obvious to "configure Chang 1's PLB 26 as Chang 1's FPGA to manipulate the signals of the Chang 1's conventional functional blocks . . . because it would enable Chang 1 to have more control of the micro-controller in manipulating the data present on Chang 2's bus interface 26," Applicant must respectfully disagree. Chang 1 is an ASIC, and Chang 2 specifically states that "[t]he simplicity and speed with which an ASFPGA may be configured into a custom ASIC is markedly different from the long and expensive procedure required to fabricate an ASIC." Col. 3, lines 42-44. Chang 1 and Chang 2 are not complementary, and the comments in Chang 2 teach against combining the references. Furthermore, Chang 2 does not a debug client function that observes and manipulates the at least one bus, rather the FPGA of Chang 2 performs logic functions necessary for operation of the ASFPGA, whatever functionality it is given.

Second, even if Barnett, Chang 1, and Chang 2 are combined, their combination does not succeed in creating anything greater than Barnett by itself. A combination of Barnett and Chang 1 results in Barnett emulating RISC or DSP 18 in Chang 1 and

providing a transparent window into its internal functioning, but no more. Col. 5, lines 42-44. Barnett fails to disclose that the emulator "manipulates the at least one bus and the plurality of internal signals," as recited in claim 1, because Barnett is an emulator. Again, Applicant respectfully requests that the Examiner review the position that Chang 2 discloses an FPGA that "manipulates the at least one bus," as Chang 2's FPGA is simply executing logic functions. If Chang 2 is added to Chang 1, Applicant reasons that FPGA 48 of Chang 2 would replace PLD 26 of Chang 1 and operate in a similar manner to Chang 1 without combination.

Finally, the references fail to teach or suggest all the claim limitations. As previously stated, none of the above references, either alone or in combination, teaches or suggests "a field programmable gate array (FPGA) function coupled to the at least one bus and the plurality of internal signals, the FPGA function including a debug client function that observes and manipulates the at least one bus and the plurality of internal signals," as recited by claim 1.

Applicant believes the Examiner has not made a prima facie case for obviousness with the cited art, therefore claim 1 is non-obvious and in condition for allowance.

If an independent claim is non-obvious under 35 U.S.C. 103, then any claim depending therefrom is non-obvious. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988). Claims 2-8 depend from claim 1, therefore claims 2-8 are also non-obvious and in condition for allowance.

Claim 9:

The debug client function with an ASIC and a FPGA is rejected as per claim 1. The modification of Chang1's PLB 26 with Barnett's FPGA to include the debug

function is presented in the rejection of claim 1. Also, the limitation of "selector logic coupled to the at least one bus and the plurality of internal signals" is rejected per claim 1.

Chang1 does not explicitly teach PLB 26 includes an external communication logic function for receiving and transmitting information to a server, however, Chang1 does suggest that the PLB 26 can implement one or more functions that is performed by the functional blocks included in the PCIBC 10, one being a PCT bus interface block 22. (Col. 5, lines 65-67; col. 6, lines 1-5). Chang1 also teaches a CPU (not illustrated in any of the FIGS.), that is included in the computer system (server), communicates with the RISC processor or DSP block 18 (also a micro-controller, programmed into the PLB 26 per Barnett, claim 1) through the PCT bus interface block 22 (Also programmed into the PCB 26). An in-system programming *"ISP") interface 28, included in the PLB 26, provides a port through which the PLB 26 may be programmed or configured (debug client function programmed by a server). (Col. 6, lines 35-45). It would have been obvious to one of the ordinary skill in the art at the time the invention was made that Chang1's PLB 26 could be programmed to implement the function of the PCI bus interface block 22 (external communication logic function). The artisan would be motivated to do so because this would enable the debug client function programmed in the PCB 26 (per Barnett) to communicate with the server.

Chang1 does not explicitly teach PLB 26 includes an interface logic, however, Chang 1 does suggest that the PLB 26 can implement one or more functions that is performed by the functional blocks included in the PCIBC 10. (Col. 5, lines 65-67; col. 6, lines 1-5). Chang2 teaches that the FPGA 48 may also be configured to perform additional logic functions (interface logic). (Col. 6, line 19-35) It would have been obvious to one of ordinary skill in the art at the time the invention was made that Chang1's PLB 26 could be programmed to implement Chang2's additional logic functions (interface logic). The artisan would be motivated to do so because this would enable Chang1 to create additional logic to interface between Chang2's bus selector circuit and Chang1's PCI bus interface block 22 (external communication logic function).

Although claim 9 differs from claim 1, the same arguments with respect to claim 1 apply to claim 9. Claim 9 is non-obvious with respect to the cited art and in condition for allowance.

Claims 10-15 depend from claim 9, therefore claims 10-15 are also non-obvious and in condition for allowance.

In view of the foregoing, Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

SAWYER LAW GROUP LLP

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Date

Michael R. Johnson
Reg. No. 55,306
(650) 493-4540